

REMARKS

The present application was filed on July 23, 2001 with claims 1-29. Claims 18-25 were withdrawn from consideration as being drawn to a non-elected invention. Claims 30 and 31 were added in an Amendment dated September 27, 2002. In the Advisory Action dated May 13, 2003, the Examiner: (i) indicated that Applicant's prior response dated April 16, 2003 has overcome the rejection of claims 3-5, 10-12, 30 and 31 under 35 U.S.C. §103(a); (ii) indicated that claims 3-5 and 10-12 are objected to; and (iii) indicated that claims 30 and 31 are allowed.

In this response, claims 1 and 26-29 have been canceled without prejudice. Additionally, Applicant amends claims 2, 3, 6-8 and 15-17 to recast the allowable subject matter into independent form and to correct the dependency of certain claims. No new matter has been entered and Applicant asserts that the above amendments do not raise new issues that require further consideration and/or search. Applicant respectfully requests reconsideration of the present application in view of the above amendments and the following remarks.

Specifically, claim 3 has been amended to recast the allowable subject matter into independent form. Additionally, claims 2, 6-8 and 15-17, all of which formerly depended from claim 1 (now cancelled), have been amended to depend from allowed claim 30.

In view of the foregoing, Applicant believes that claims 2-17, 30 and 31 are in condition for allowance, and respectfully requests withdrawal of the §102(e) and §103(a) rejections.

Attached hereto is a marked-up version of the changes made to the claims by the present Amendment. The attachment is captioned "Version with Markings to Show Changes Made."

Respectfully submitted, ✓



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 1 and 26-29 have been canceled without prejudice.

Claims 2, 3, 6-8 and 15-17 have been amended by rewriting same as follows:

2. (Amended) The integrated circuit of claim [1] 30, further comprising:

a plurality of conductive plugs formed in the substrate, the plugs providing a substantially low resistance path for electrically connecting the conductive layer to the isolation buried layer.

3. (Amended) [The integrated circuit of claim 1,] An integrated circuit, comprising:

a first circuit section formed in a substrate;

a second circuit section formed in the substrate, the second circuit section being spaced laterally from the first circuit section;

an isolation buried layer formed under at least a portion of the first circuit section; and

a conductive layer formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer at a plurality of points spaced throughout the buried layer, the conductive layer reducing an effective lateral resistance of the isolation buried layer to thereby increase an electrical isolation between the first and second circuit sections;

wherein the conductive layer comprises[:] a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net.

6. (Amended) The integrated circuit of claim [1] 30, wherein the isolation buried layer is connected to a ground or reference source.

7. (Amended) The integrated circuit of claim [1] 30, wherein the conductive layer is formed at least in part of metal.

8. (Amended) The integrated circuit of claim [1] 30, further comprising:

a second isolation buried layer formed under at least a portion of the second circuit section; and

a second conductive layer formed on a surface of the integrated circuit and operatively coupled to the second isolation buried layer, the second conductive layer reducing an effective lateral resistance of the second isolation buried layer.

15. (Amended) The integrated circuit of claim [1] 30, wherein:

the integrated circuit is a mixed signal integrated circuit;

the first circuit section comprises a digital circuit section; and

the second circuit section comprises an analog circuit section.

16. (Amended) The integrated circuit of claim [1] 30, wherein the isolation buried layer has a lower resistivity than the substrate.

17. (Amended) The integrated circuit of claim [1] 30, wherein the isolation buried layer is formed in the substrate at depth in a range from about 2 micrometers (μm) to about 5 μm from an upper surface of the substrate.